IN THE CLAIMS:

Please note that, pursuant to 37 CFR 1.121(c)(3), all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity and for the convenience of the Patent Office. Also attached is a version with markings to show changes made to the claims.

Please cancel claim 14 without prejudice or disclaimer

Please amend claim 1 as set forth below.

1. (Twice Amended) An integrated circuit package comprising:

a semiconductor die;

a lead frame including a plurality of conductors, at least some of which are coupled to the semiconductor die;

insulating material encompassing the semiconductor die and at least a portion of the lead frame; and

at least one alignment feature formed in the lead frame separate from the plurality of conductors and at least partially external to the insulating material, the at least one alignment feature being configured to facilitate positive alignment of the integrated circuit package with an external structure and wherein the at least one alignment feature is configured to be removable from the integrated circuit package.

2. The integrated circuit package of claim 1, wherein the at least one alignment feature includes at least one aperture.

3. (Previously Amended) The integrated circuit package of claim 1, wherein the at least one alignment feature is semicircular shaped.

4. (Previously Amended) The integrated circuit package of claim 1, wherein the integrated circuit package includes a first end and a second end, and wherein the at least one alignment feature comprises an alignment feature disposed on both the first end and the second end of the integrated circuit package.

5. The integrated circuit package of claim 1, wherein the at least one alignment feature comprises a protuberance.

6. (Previously Amended) An integrated circuit package comprising:

a semiconductor die;

a lead frame including a plurality of conductors, at least some of which are coupled to the semiconductor die;

at least one alignment feature formed in the lead frame separate from the conductors and configured to facilitate positive alignment of the integrated package with an external structure; and

insulating material encompassing the semiconductor die and the at least one alignment feature, the insulating material being bound by a peripheral edge, wherein the alignment feature is formed and encompassed along the peripheral edge.

7. (Previously Amended) The integrated circuit package of claim 6, wherein the at least one alignment feature is an alignment cut out.

9. (Previously Amended) The integrated circuit package of claim 6, wherein the at least one alignment feature is semicircular shaped.

10. The integrated circuit package of claim 6, wherein the at least one alignment feature comprises a tie bar.

11. (Previously Amended) The integrated circuit package of claim 6, wherein the lead frame includes a first end and a second end, wherein the at least one alignment feature comprises an alignment feature disposed on both the first end and the second end of the lead frame.

12. The integrated circuit package of claim 6, wherein the at least one alignment feature comprises a protuberance.

13. (Previously Amended) A lead frame strip ready for cutting, the lead frame strip comprising a plurality of integrated circuit packages, each integrated circuit package comprising:

a semiconductor die;

a lead frame including a plurality of conductors, at least some of which are coupled to the semiconductor die;

insulating material encompassing the semiconductor die and portions of the plurality of conductors; and

at least one alignment feature formed in a portion of the lead frame separate from the conductors and electrically isolated from the plurality of conductors.

15. The integrated circuit package of claim 6, wherein the at least one alignment feature is configured to be removable from the integrated circuit package.

16. The lead frame strip of claim 13, wherein the at least on alignment feature is configured to be removable from its respective integrated circuit package.